CALL FOR TUTORIALS

DVCON US 2021

March 1-4, 2021 • Virtual

2021 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCon is the premier conference on the application of languages, tools, and methodologies for the design and verification of electronic systems and integrated circuits. The focus of the conference is the usage of specialized design and verification languages such as Verilog, SystemVerilog, VHDL, PSL, SystemC and e, as well as general purpose languages such as C, C++, Perl, Tcl, and Python. Tools and methodologies include the use of machine learning, open-source software, hardware and architecture, testbench automation, hardware-assisted verification, hardware/software co-verification, formal verification, transaction-level system design, high level synthesis, low power design techniques, 3D chip designs, IP based SoC design methods, reference flows and AMS design.

DVCon is seeking tutorial topics that are current, have a high-level of interest and offer strong continuing educational content.

Tutorial sponsors reach a captive audience during the 2 hrs of educational sessions and have the opportunity to follow-up with them during breaks, at the exhibits, and following the event.

DVCon is a highly targeted venue for engineers addressing major design and verification issues. You can position your company at the forefront of these discussions by sponsoring either of the Tutorials listed below. Submit proposals by **Tuesday, September 22.** For suggested topics and timeline, see page 2.

Submit Here: 2021.dvcon.org/call-tutorials

DVCON SPONSORED TUTORIAL: $3,000

Sponsorship Includes:

- 2 hours Presentation
- 1 dedicated email distribution to the DVCon mail list
- Your company logo will be displayed on the conference website & in PDF program
- Recognition during Opening Ceremony
- Copy of the 2021 Session Attendee List w/ Emails
  (We will share lists of attendees who have given us permission to do so.)

Sponsored tutorials will be reviewed and approved by the program committee with respect to technical depth and applicability. In case of multiple organizations presenting a sponsored tutorial only the organizing company would get the sponsorship benefits mentioned above.

For more information concerning the conference, please contact the conference management,
Laura LeBlanc at lleblanc@conferencecatalysts.com

Detailed guidelines for preparing the presentations will be made available after selections are final.

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TUTORIAL PROPOSAL REQUIREMENTS

Deadline: September 22, 2020

DVCon tutorials are open to all attendees and are included in the full conference registration. Please include in the proposal the name of the companies that will be sponsoring the tutorial.

- Attendee expectations are high regarding currency of topic, depth of engineering content and breadth of real-life examples
- The Tutorial Chair will review final presentation materials to ensure high quality educational content
- Include suggested presenters names, affiliations & biographies
- Your proposal should be a short abstract of the tutorial, two to five paragraphs, 1,000 words maximum
- Presentation slides need to be supplied in an electronic format in advance of the conference. Presentation slides will be distributed to the attendees in electronic format. Hard copies will not be provided
- Please indicate if this tutorial is a "hands-on" session or lecture format
- Any necessary additional hardware that you may require must be provided by the tutorial organizers

SUGGESTED TOPICS

DVCon tutorials are open to all attendees and are included in the full conference registration. Please include in the proposal the name of the companies that will be sponsoring the tutorial.

- SystemVerilog for Verification and/or Design
- SystemC /C/C++ Design and/or Verification of systems.
- SoC and Software-driven Verification
- Assertion-based Verification. SystemVerilog Assertions, PSL, etc.
- Coverage-driven Verification
- High-level Synthesis
- Low-power Design and Verification techniques
- Secure/Encrypted IP-based SoC design methods
- Debug for design and verification
- Mixed-signal modeling and verification
- Transaction Level Modeling (TLM), ESL Design, and IP integration (IP-XACT)
- Functional Safety
- Security
- Embedded software verification
- Hardware/Software Co-development
- Verification Productivity Methods
- Formal Methodology and Static Analysis
- Emulation
- Post SI Debug
- FPGA Prototyping
- Moving from proprietary solutions to standards-based design and verification
- Portable Stimulus
- Machine Learning driven techniques
- Open source hardware/software/architecture

TUTORIAL DEADLINES

September 22, 2020: Proposals due. Submit at DVCon.org

November 3, 2020: Accept/Reject notification

November 25, 2020: All Tutorial content due for Conference Program and website: tutorial title, abstract, speaker names, affiliations and biographies

January 7, 2021: Draft Presentation slides due to DVCon Tutorial Chair

January 19, 2021: Presentation feedback due to presenters on slides

February 9, 2021: Final slides due for final production for attendee distribution

CONFERENCE SCHEDULE

Monday, March 1:
- Accellera Day Tutorials
- Short Workshops
- Exhibits

Tuesday, March 2:
- Technical Sessions
- Keynote Speaker
- Poster Session
- Exhibits

Wednesday, March 3:
- Technical Sessions
- Panel Discussions
- Exhibits

Thursday, March 4:
- Tutorials
- Short Workshops

Conference Sponsor:

accellera SYSTEMS INITIATIVE

General Chair
Aparna Dey, *Cadence Design Systems, Inc.*
aparna@cadence.com

Tutorial Chair
Ambar Sarkar, *NVIDIA Corp*
ambars@nvidia.com

Accellera Systems Initiative is an industry consortium with a mission to provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process. **Accellera.org**